IN THE CLAIMS

Claims 1-37 (Canceled)

38. (Previously Presented) A data buffering unit, comprising:

a memory that includes a plurality of first-in-first-out (FIFO) memories to store data;

a memory read manager to tie assert read enable inputs of the FIFO memories and to select a first FIFO memory to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address.

39. (Previously Presented) The data buffering unit of Claim 38, wherein the memory read manager comprises a memory enable unit that asserts a read enable line to each of the plurality of FIFO memories such that the FIFO memories may always be read.

40. (Previously Presented) The data buffering unit of Claim 38, wherein the memory read manager comprises a read address manager that determines which of the plurality of FIFO memories to access in response to a read address from the data reading device.

41. (Previously Presented) The data buffering unit of Claim 38, wherein the memory read manager comprises a read selector, coupled to data outputs of each of the FIFO memories, to select an appropriate data output to receive data from in response to a read address from the data reading device.

42. (Previously Presented) The data buffering unit of Claim 38, wherein the memory read manager comprises a plurality of read pointer managers, each corresponding to one of the FIFO memories, the read pointer managers transmit an appropriate read address to each of the FIFO memories to prepare data to be prepared for output on the FIFO memories prior to receiving a request for the data from the data reading device.

43. (Previously Presented) The data buffering unit of Claim 38, further comprising a memory write manager that directs data from the data transmitting device to be written into each of the FIFO memories in a round robin fashion.

44. (Previously Presented) The data buffering unit of Claim 43, wherein the memory write manager comprises a write address manager that determines which of the FIFO memories to access in response to a write address received from the data transmitting device.

45. (Previously Presented) The data buffering unit of Claim 44, wherein the write address manager determines a write address in one of the FIFO memories to write data in response to the write address received from the data transmitting device.

46. (Previously Presented) The data buffering unit of Claim 43, wherein the memory write manager comprises a write selector that transmits a write enable signal and data from the data transmitting device to an appropriate FIFO memory in response to the work address manager.

47. (Previously Presented) A programmable logic device (PLD), comprising,

memory blocks that form comprises a plurality of first-in-first-out (FIFO) memories to store data from a data transmitting device; and

logic elements to form a memory read manager to tie assert read enable inputs of the FIFO memories and to select a first FIFO memory to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address from the data reading device.

48. (Previously Presented) The PLD of Claim 47, wherein the memory read manager comprises a memory enable unit that asserts a read enable line to each of the plurality of FIFO memories such that the FIFO memories may always be read.

49. (Previously Presented) The PLD of Claim 47, wherein the memory read manager comprises a read address manager to determine which of the plurality of FIFO memories to access in response to a read address from the data reading device.

50. (Previously Presented) The PLD of Claim 47, wherein the memory read manager comprises a read selector, coupled to data outputs of each of the FIFO memories, to select an appropriate data output to receive data from in response to a read address from the data reading device.

51. (Previously Presented) The PLD of Claim 47, wherein the memory read manager comprises a plurality of read pointer managers, each corresponding to one of the FIFO memories, the read pointer managers transmit an appropriate read address to each of the FIFO memories to prepare data to be prepared for output on the FIFO memories prior to receiving a request for the data from the data reading device.